REMARKS/ARGUMENTS

Entry of these Remarks and reconsideration of all claims remaining of record is earnestly requested. Claims 80-223 are currently pending.

By this amendment, claim 83 is canceled without prejudice or disclaimer.

Claims 80, 98 and 223 were rejected under the judicially created doctrine of obviousness-type double patenting as allegedly being unpatentable over commonly assigned U.S. Patent No. 6,646,653.

Applicants respectfully traverse this rejection for at least the following reasons:

Claims 80 and 89 require "a housing having an insertion port for a removable memory" and are directed toward rendering and displaying polygon-based 3D graphic objects. Likewise, claim 206 requires a housing for receiving a portable removable non-volatile memory and recites the rendering and displaying of polygon-based 3D graphic objects. These features are not recited in claims 1, 2 or 4 of U.S. Patent 6,646,653. Applicants respectfully contend that claims 80, 98 and 206 are patentably distinct at least because the recited features of a housing having an insertion port and the rendering of polygon-based 3D objects are not inherent to claims 1, 2 and 4 of the '653 patent and, moreover, would not be obvious from the contexts of those claims.

Re The 35 U.S.C. § 112 Second Paragraph Rejections and Claims Objections:

Claims 80-86, 88, 90-96, 98-105, 107, 109-115, 138 and 202 were objected to because of minor informalities. In addition, claims 159 and 211 were rejected under 35 U.S.C. § 112, second paragraph, as lacking antecedent basis for the phrase "the circuitry". By this amendment, Applicants have amended the above listed claims to obviate the Examiner's rejections and objections, and to more clearly set forth and distinctly claim Applicants invention.

Re The 35 U.S.C. § 112 First Paragraph Rejections:

Claims 85, 88, 92, 98-205, 207, 214 and 218 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Applicants respectfully traverse this rejection and contend that the subject matter of the above claims is adequately described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors had possession of the claimed invention at the time the invention was filed, as evidenced and supported by at least by the following portions of Applicants' specification as originally filed:

Regarding the rejection of claims 98, 135, 154 and 186, Applicants submit that the specification adequately describes a "game program processing unit for executing at least a portion of a video graphics program that includes instructions for displaying polygon-based 3D objects", as evidenced by at the least following passages in Applicants' specification:

- "...In an exemplary embodiment described herein, the present invention is embodied in a video game system including a host video game system and a video game cartridge housing the graphics microprocessor" (Applicants' specification at page 4, lines 25 et seq.)
- Applicants' specification at page 5, lines 1 et seq. (describing a video game system and a host microprocessor). See also page 5 at lines 17-21 and page 7 at lines 22 et seq.
- Applicants' specification at page 121, lines 20 et seq.
- Applicants' specification at page 24, lines 1 et seq. and Figure 2, block 20.

- Applicants' specification at page 121, lines 20 et seq. and Figure 18. In particular, see page 121, lines 20-25 and lines 21-30.

Regarding the rejection of claims 117, 172, 187, 202 and 204, Applicants submit that the specification adequately describes a "game program processor", as understood from the context of those claims, as evidenced in at least the following passages:

- Applicants' specification at page 135, lines 1-5 (the "...host computer system, e.g., the Super NES is an example of a game program processor").
- Applicants' specification at page 24, lines 1 et seq. and lines 11 et seq. with reference to Figure 2 and CPU 22, "which is representative of the Super NES game program system sold by Nintendo of America."

Regarding the rejection of claims 85, 103, 122-124, 141, 154, 174 and 192, Applicants submit that the specification adequately describes "a graphic processor including graphics geometry transformation circuitry for performing rotation and or scaling of a 3D graphic object or portions of the object to be displayed", as evidence by at least the following portions of the specification:

- Applicants' specification at page 121, lines 20 et seq. and Figure 18.
- Applicants' specification at page 135, lines 11 et seq. which describe a graphic coprocessor which "may be used to generate 3D type (and other) special effects including those involving rotated and scaled polygon-based objects at high speed..."; See also Figure 1 and Figures 4A and 4B.

Applicants also submit that the specification adequately describes the graphics geometry transformation circuitry and what it includes, as evidenced at least by:

- Applicants' specification at pages 17, lines 3 et seq. with reference to Figures 1, 4A and 4B.

Applicants submit that it is readily understandable from the content of the specification in at least the above passages that the claimed graphics geometry transformation circuitry refers to the example circuitry of Figures 4a and 4b. For example, see Applicants' specification at page 33, lines 12-23 (regarding "hardware" 52) and lines 24 et seq., page 34, lines 3 et seq., page 35, lines 4 et seq. and page 35, lines 21-23.

Regarding the rejection of claims 88, 107, 125, 144, 162, 176, 195 and 214, Applicants submit that the specification adequately describes "an array of data corresponding to polygon vertex points that are rotated by programming the graphics processor", as evidenced at least by the following:

- Applicants' specification at page 130, lines 13-19 and the example program listing for rotating an array of X, Y and Z points, as disclosed at pages 131-134. (wherein the X, Y and Z points define 3D graphic geometry pertaining to, for example, verticies of a 3D object).

Regarding the rejection of claims 92, 111, 129, 148, 166, 180, 199 and 218, Applicants submit that the specification adequately describes a home video game system including a set of instructions for programming the graphics processor unit for rendering 3D objects, as evidenced at least by the following:

- Applicants' specification at page 121, lines 20 et seq. through page 123, lines 16 (which disclose a program for generation of a polygon). The set of "instructions" may include, for example, the set of instructions described at pages 71-76. See also the program listing at pages 131-134 for rotating an

array of X, Y, Z points (which for example, describe the spacial coordinates of the verticies of one or more 3D polygons).

Regarding the rejection of claim 117, Applicants submit that the specification adequately describes the graphics processor including a programmable processor having embedded RAM cache memory, as evidenced at least by the following:

- Applicants' specification at page 17, lines 15-18 and block 2 in Figure 1, Figure 4A and Figure B. See also page 104, lines 3 et seq. and 12 et seq. (The Mario chip graphics processor is a "programmable processor").
- Applicants' specification at Figure 4B depicts embedded RAM cache memory at block 94 labeled "cache RAM". In particular, see Applicants' specification at page 41, lines 4 et seq. through page 42, line 25.
- Applicants' specification at page 105, line 24 et seq. discusses loading Mario chip graphics processor's cache RAM with program instructions: "....controls in part the loading of the *Mario chip cache RAM 94 with currently executing program instructions...*" (emphasis added) and "Instructions are loaded into cache RAM 94 in 16-byte groupings." See also page 106, lines 5 et seq.

Regarding the rejections of claim 118, Applicants submit that the specification adequately describes instructions used for rendering 3D objects that the coprocessor is responsive to, as evidenced at least by the following:

- Applicants' specification at, for example, lines 20 et seq. through page 123 (disclosing an example program for generating a polygon) and pages 131-134 (disclosing an example program for rotating an array of X, Y, Z points).

Re The 35 U.S.C. § 103 Rejections:

Claims 80, 135 and 206 were rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent 5,016,876 to Loffredo in view of U.S. Patent 5,190,285 to Levy et al. Applicants respectfully traverse this rejection. The Office Action alleges that the Loffredo '876 patent (with reference to Figure 1) discloses a programmable graphics processor ("a digital computer 22") and a main processor ("DMA coprocessor 130") that communicates information relating to one or more polygon-based 3D graphic objects to the programmable graphics processor. The Office Action further alleges that Loffredo '876 also discloses that the graphics processor is programmed to render at least one or more portions of said 3D polygon-based graphic objects for display on the display device. (See 6/15/05 Office Action at page 10).

Applicants respectfully contend that, among other things, the Loffredo '876 reference does not show or suggest the rendering of polygon-based 3D graphic objects for display, as set forth in applicants' claims. Instead, the Loffredo '876 patent is directed toward a DMA co-processor (130) "especially adapted for providing real-time animation of the image data." (See '876 patent at Abstract and Figure 1.) Although, the Office Action attempts to read Loffredo's DMA coprocessor (130) on Applicants' claimed "main processor", Applicants contend that Loffredo's DMA coprocessor (130) will not function as "main processor".

In addition, there is no teaching or suggestion by Loffredo that the main processor (identified by the Office Action as "DMA coprocessor 130") communicates information relating to *polygon-based* 3D graphic objects to the programmable graphics processor (identified by the Office Action as "digital computer 22"). Moreover, there is no teaching or suggestion by Loffredo that a programmable graphics processor ("digital computer 22") is programmed to render *polygon-based* 3D graphics. Although the Office Action identifies portions of the '876

patent specification to support the rejection (to wit, col. 9, lines 23-38 and col. 1, lines 50-60), these referenced sections only discuss the possibility of creating a *composite scene* by "overlaying successive planes of image data" that are read from an image memory. Nowhere in the '876 patent does Loffredo discuss the generating or displaying of polygon-based 3D graphics. Moreover, there is no mention or suggestion in the '876 patent of providing programming for rendering polygon-based 3D graphics.

The Levy et al. ('285) reference is applied as allegedly disclosing a removable memory storage device ("external unit 92"). (The Office Action admits that Loffredo does not explicitly disclose a removable memory storage device.) The Office Action alleges that "it would have been obvious to one of ordinary skill in the art at the time of the invention to substitute the memory storage of Loffredo with the removable memory as taught by Levy to improve the video game by permitting existing processor to address a larger program memory address space." Although Applicants respectfully contend that there is no teaching by either Levy or Loffredo that suggests the obviousness of modifying the Loffredo device to operate with a removable memory, even assuming for the sake of argument that this feature of the Levy reference were properly applicable to Loffredo '876, the Levy et al. reference does not remedy the deficiencies of Loffredo with respect to the claimed rendering of polygon-based 3D graphic objects. Neither Levy et al. nor Loffredo teach or suggest the rendering of polygon-based 3D graphic objects as set forth in Applicants' claims.

When a rejection depends on a combination of prior art references, there must be some teaching, suggestion, or motivation to combine the references. See In re Geiger, 815 F. 2d 686, 688, 2 USPQ2d 1276, 1278 (Fed. Cir. 1987).

Accordingly, it is submitted that claims 80, 135 and 206 and the claims dependent thereon are patentably distinct over the combined teachings of Loffredo and Levy et al.

Claims 81-134, 136-205 and 207-223 were rejected under 35 U.S.C. §103(a) as being unpatentable over the Loffredo '876 patent in view of the Levy et al. '285 patent and further in view of a PC TECH Journal publication by McNierney. Applicants respectfully traverse this rejection.

The McNierney reference is cited for its review of the Texas Instruments TMS34010 processor architecture, which the Office Action (not the McNierney article) alleges is "responsive to specific instructions used for rendering 3D objects." (See 6/15/05 Office Action, page 11.) However, there is no discussion or suggestion by McNierney of using the TMS processor for generating polygon-based 3D graphic objects as set for the in Applicants' claims. At best, McNierney lists only a few graphics instructions enabling pixel copying, pixel block transfers and line drawing, and only one instruction ("FILL") that enables one to "[f]ill a rectangle defined by the DYDX (delta-*y*/delta-*x*) register using the color in the COLOR1 register." There is no discussion of 3D graphics related instructions (e.g., shading, rotating, scaling, etc.) or suggestion of using the FILL instruction for rendering 3D graphic objects. There is no mention of any other polygon primitives (e.g., triangles) or of polygon related instructions or programming for manipulating polygon vertices as would be appropriate and necessary for teaching or suggesting polygon-based rendering of 3D graphic objects.

As previously explained above, neither Levy et al. nor Loffredo teach or suggest the rendering of polygon-based 3D graphic objects. For at least the reasons stated immediately above, Applicants' respectfully contend that McNierney does not remedy the deficiencies of Levy et al. and Loffredo with respect to the rendering of polygon-based graphic objects.

As such, the proposed combination of Levy et al., Loffredo and McNierney would not have taught or suggested the rendering of polygon-based 3D graphic objects as set forth in Applicants' claims 81-134, 136-205 and 207-223. Moreover, at least with respect to Applicants' independent method claims 186, 202 and 204, neither Levy et al. nor Loffredo, nor McNierney teach or suggest steps for producing graphics display effects utilizing rotated and/or scaled polygon-based graphic objects, as set forth in those claims.

Consequently, since claims 81-97, 99-116, 118-134, 136-153, 155-171, 173-185, 187-201, 203, 205 and 207-223 are dependent on independent claims 80, 98, 117, 135, 154, 172, 186, 202, 204 and 206, and since neither Levy et al., nor Loffredo, nor McNierney suggest the features or steps as discussed above and set forth in Applicants' independent claims, it is respectfully submitted that all of Applicants' dependent claims are patentable over the combined teachings of these references.

In view of Applicant's foregoing remarks, it is believed that the application is in condition for allowance. Favorable consideration and allowance of this application are respectfully solicited. If any small manner remains outstanding, the Examiner is encouraged to telephone Applicants' representative at the telephone number listed below or on the following page.

Respectfully submitted,

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